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Kind regards,

Team Nexperia

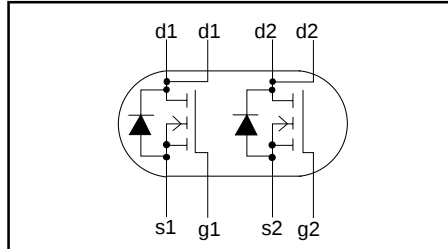
Dual N-channel enhancement mode TrenchMOS™ transistor

PHN210

FEATURES

- Dual device
- Low threshold voltage
- Fast switching
- Logic level compatible
- Surface mount package

SYMBOL



QUICK REFERENCE DATA

$V_{DS} = 30 \text{ V}$
$I_D = 3.4 \text{ A}$
$R_{DS(ON)} \leq 100 \text{ m}\Omega \text{ (} V_{GS} = 10 \text{ V)}$
$R_{DS(ON)} \leq 200 \text{ m}\Omega \text{ (} V_{GS} = 4.5 \text{ V)}$

GENERAL DESCRIPTION

Dual N-channel enhancement mode field-effect transistor in a plastic envelope using 'trench' technology.

Applications:-

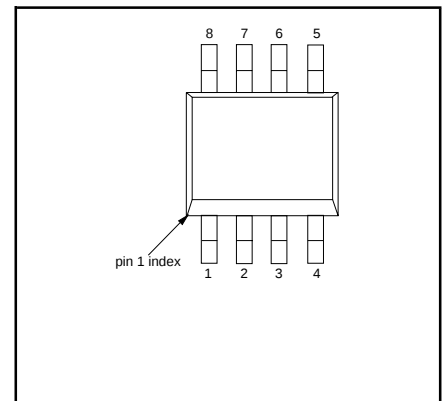
- Motor and relay drivers
- d.c. to d.c. converters
- Logic level translator

The PHN210 is supplied in the SOT96-1 (SO8) surface mounting package.

PINNING

PIN	DESCRIPTION
1	source 1
2	gate 1
3	source 2
4	gate 2
5,6	drain 2
7,8	drain 1

SOT96-1



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Repetitive peak drain-source voltage	$T_j = 25^\circ\text{C to } 150^\circ\text{C}$	-	30	V
V_{DS}	Continuous drain-source voltage		-	30	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	30	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Drain current per MOSFET ¹	$T_a = 25^\circ\text{C}$	-	3.4	A
		$T_a = 70^\circ\text{C}$	-	2.8	A
I_D	Drain current per MOSFET (both MOSFETs conducting) ¹	$T_a = 25^\circ\text{C}$	-	2.4	A
		$T_a = 70^\circ\text{C}$	-	1.9	A
I_{DM}	Drain current per MOSFET (pulse peak value)	$T_a = 25^\circ\text{C}$	-	14	A
P_{tot}	Total power dissipation (either or both MOSFETs conducting) ¹	$T_a = 25^\circ\text{C}$	-	2	W
		$T_a = 70^\circ\text{C}$	-	1.3	W
T_{stg}, T_j	Storage & operating temperature		- 65	150	$^\circ\text{C}$

¹ Surface mounted on FR4 board, $t \leq 10 \text{ sec}$

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THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-a}$	Thermal resistance junction to ambient	Surface mounted, FR4 board, $t \leq 10$ sec	-	62.5	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	Surface mounted, FR4 board	150	-	K/W

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy (per MOSFET)	Unclamped inductive load, $I_{AS} = 3.4$ A; $t_b = 0.2$ ms; T_j prior to avalanche = 25°C ; $V_{DD} \leq 15$ V; $R_{GS} = 50\ \Omega$; $V_{GS} = 10$ V	-	13	mJ
I_{AS}	Non-repetitive avalanche current (per MOSFET)		-	3.4	A

ELECTRICAL CHARACTERISTICS

 $T_j = 25^\circ\text{C}$, per MOSFET unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$ V; $I_D = 10\ \mu\text{A}$; $T_j = -55^\circ\text{C}$	30 27	- -	- -	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1$ mA $T_j = 150^\circ\text{C}$ $T_j = -55^\circ\text{C}$	1 0.4 -	2 - -	2.8 - 3.2	V V V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 2.2$ A $V_{GS} = 4.5$ V; $I_D = 1$ A $V_{GS} = 10$ V; $I_D = 2.2$ A; $T_j = 150^\circ\text{C}$	- - -	80 120 -	100 200 170	m Ω m Ω m Ω
g_{fs}	Forward transconductance	$V_{DS} = 20$ V; $I_D = 2.2$ A	2	4.5	-	S
$I_{D(ON)}$	On-state drain current	$V_{GS} = 10$ V; $V_{DS} = 1$ V; $V_{GS} = 4.5$ V; $V_{DS} = 5$ V	3.5 2	- -	- -	A A
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 24$ V; $V_{GS} = 0$ V; $V_{DS} = 24$ V; $V_{GS} = 0$ V; $T_j = 150^\circ\text{C}$	- -	10 0.6	100 10	nA μA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 20$ V; $V_{DS} = 0$ V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	$I_D = 2.3$ A; $V_{DD} = 15$ V; $V_{GS} = 10$ V	-	6	-	nC
Q_{gs}	Gate-source charge		-	0.7	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	0.7	-	nC
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 20$ V; $R_D = 18\ \Omega$; $V_{GS} = 10$ V; $R_G = 6\ \Omega$	-	6 8	- -	ns ns
t_r	Turn-on rise time		-	21	-	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	15	-	ns
t_f	Turn-off fall time		-	-	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0$ V; $V_{DS} = 20$ V; $f = 1$ MHz	-	250	-	pF
C_{oss}	Output capacitance		-	88	-	pF
C_{rss}	Feedback capacitance		-	54	-	pF

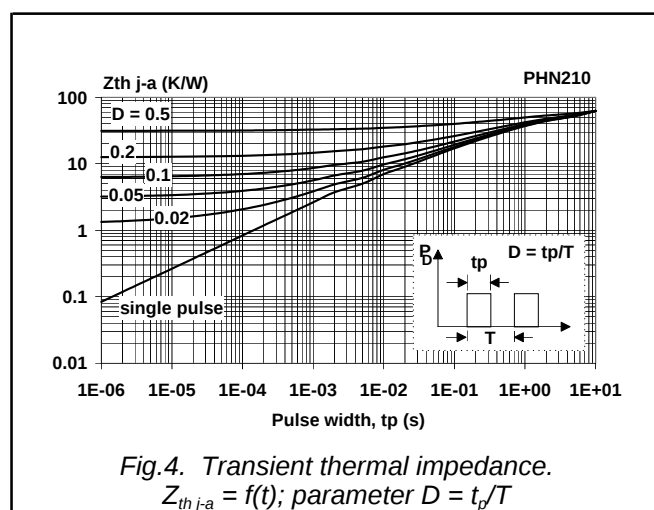
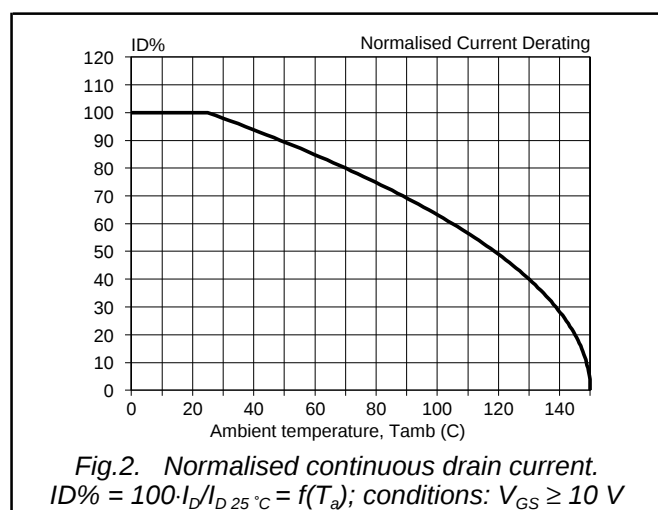
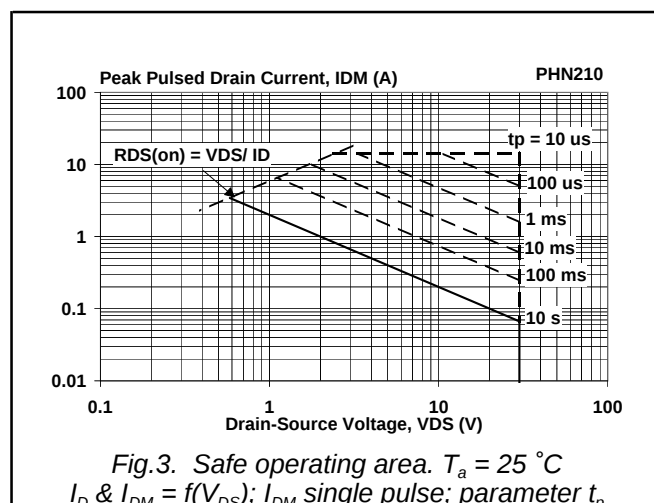
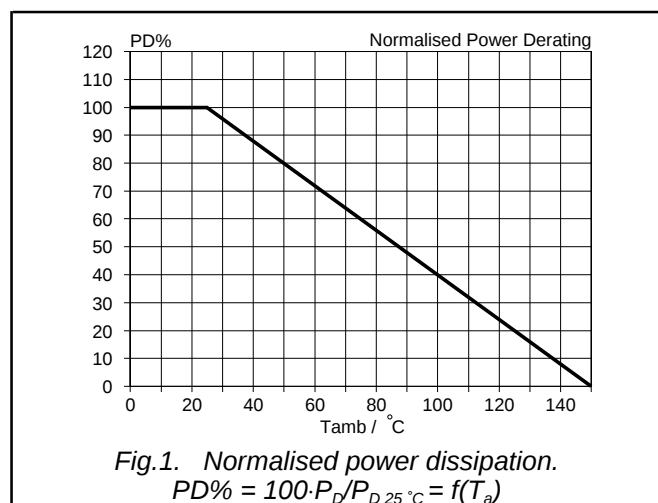
Dual N-channel enhancement mode TrenchMOS™ transistor

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REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j = 25^\circ\text{C}$, per MOSFET unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source diode current (per MOSFET)	$T_a = 25^\circ\text{C}$	-	-	2.2	A
I_{SM}	Pulsed source diode current (per MOSFET)		-	-	14	A
V_{SD}	Diode forward voltage	$I_F = 1.25\text{ A}$; $V_{GS} = 0\text{ V}$	-	0.82	1.2	V
t_{rr}	Reverse recovery time	$I_F = 1.25\text{ A}$; $-dI_F/dt = 100\text{ A}/\mu\text{s}$;	-	69	-	ns
Q_{rr}	Reverse recovery charge	$V_{GS} = 0\text{ V}$; $V_R = 25\text{ V}$	-	55	-	nC



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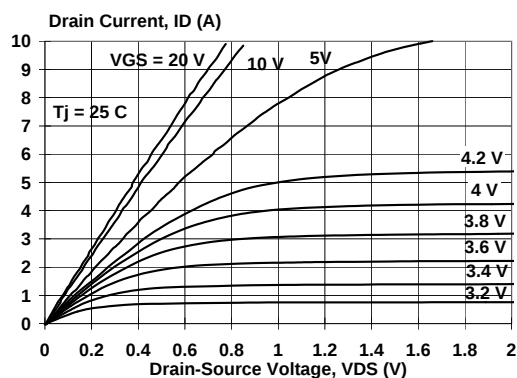


Fig. 5. Typical output characteristics, $T_j = 25\text{ }^{\circ}\text{C}$.
 $I_D = f(V_{DS})$; parameter V_{GS}

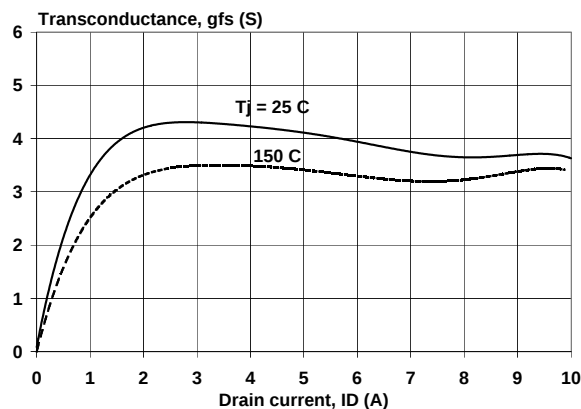


Fig. 8. Typical transconductance, $T_j = 25\text{ }^{\circ}\text{C}$.
 $g_{fs} = f(I_D)$; parameter T_j

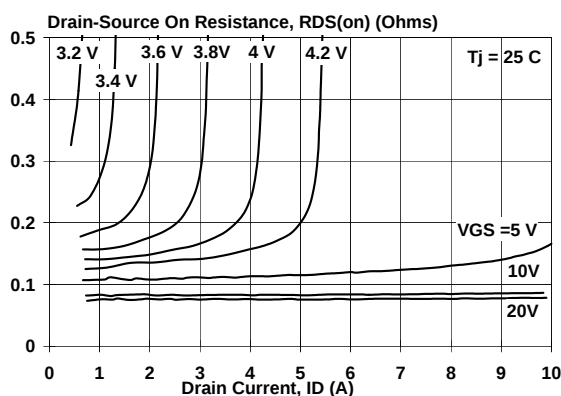


Fig. 6. Typical on-state resistance, $T_j = 25\text{ }^{\circ}\text{C}$.
 $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

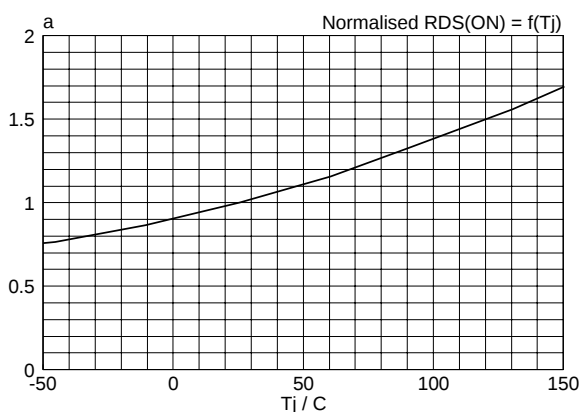


Fig. 9. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25\text{ }^{\circ}\text{C}} = f(T_j)$

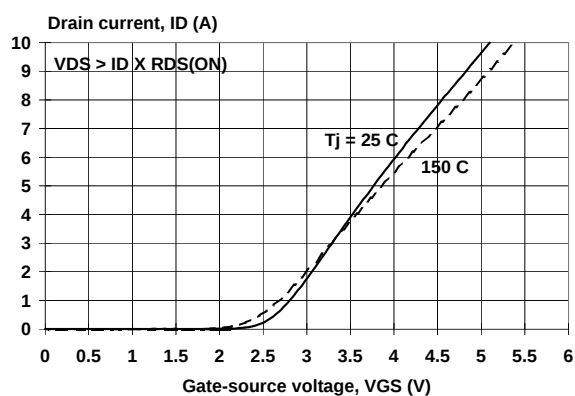


Fig. 7. Typical transfer characteristics.
 $I_D = f(V_{GS})$; parameter T_j

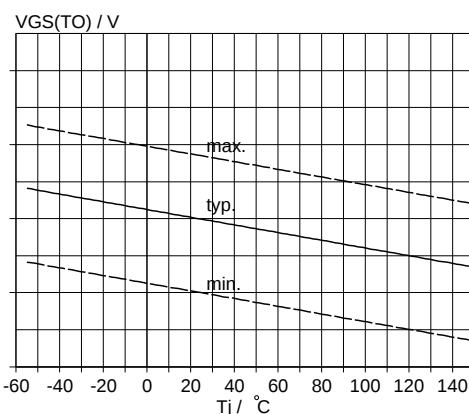


Fig. 10. Gate threshold voltage.
 $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

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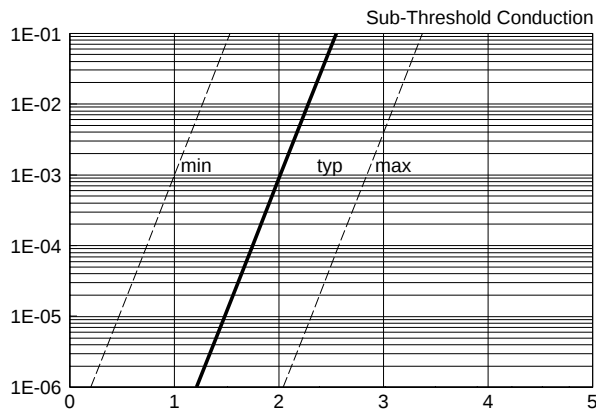


Fig.11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_J = 25^\circ\text{C}$; $V_{DS} = V_{GS}$

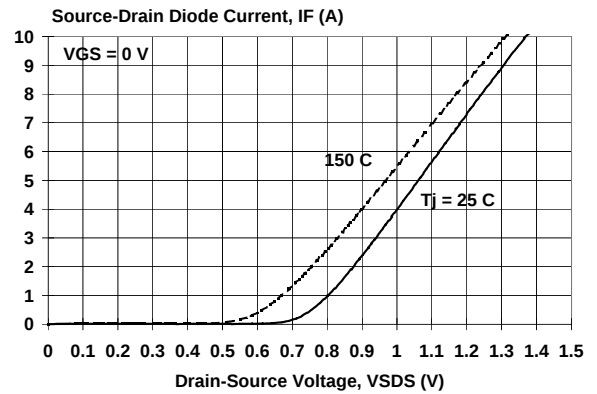


Fig.14. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0\text{ V}$; parameter T_J

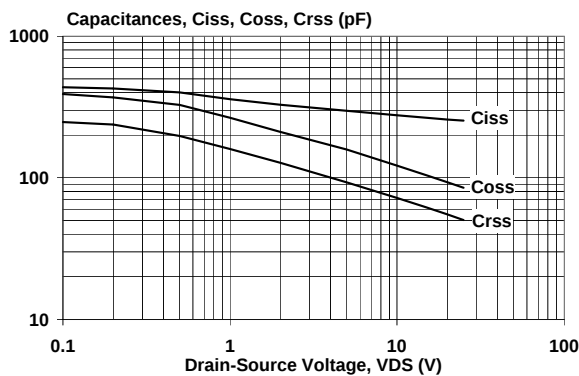


Fig.12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

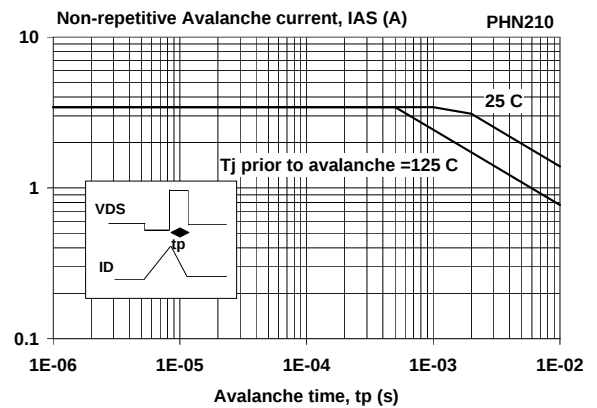


Fig.15. Maximum permissible non-repetitive avalanche current (I_{AS}) versus avalanche time (t_p); unclamped inductive load

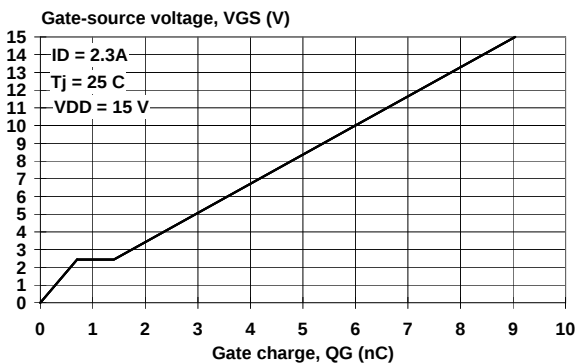
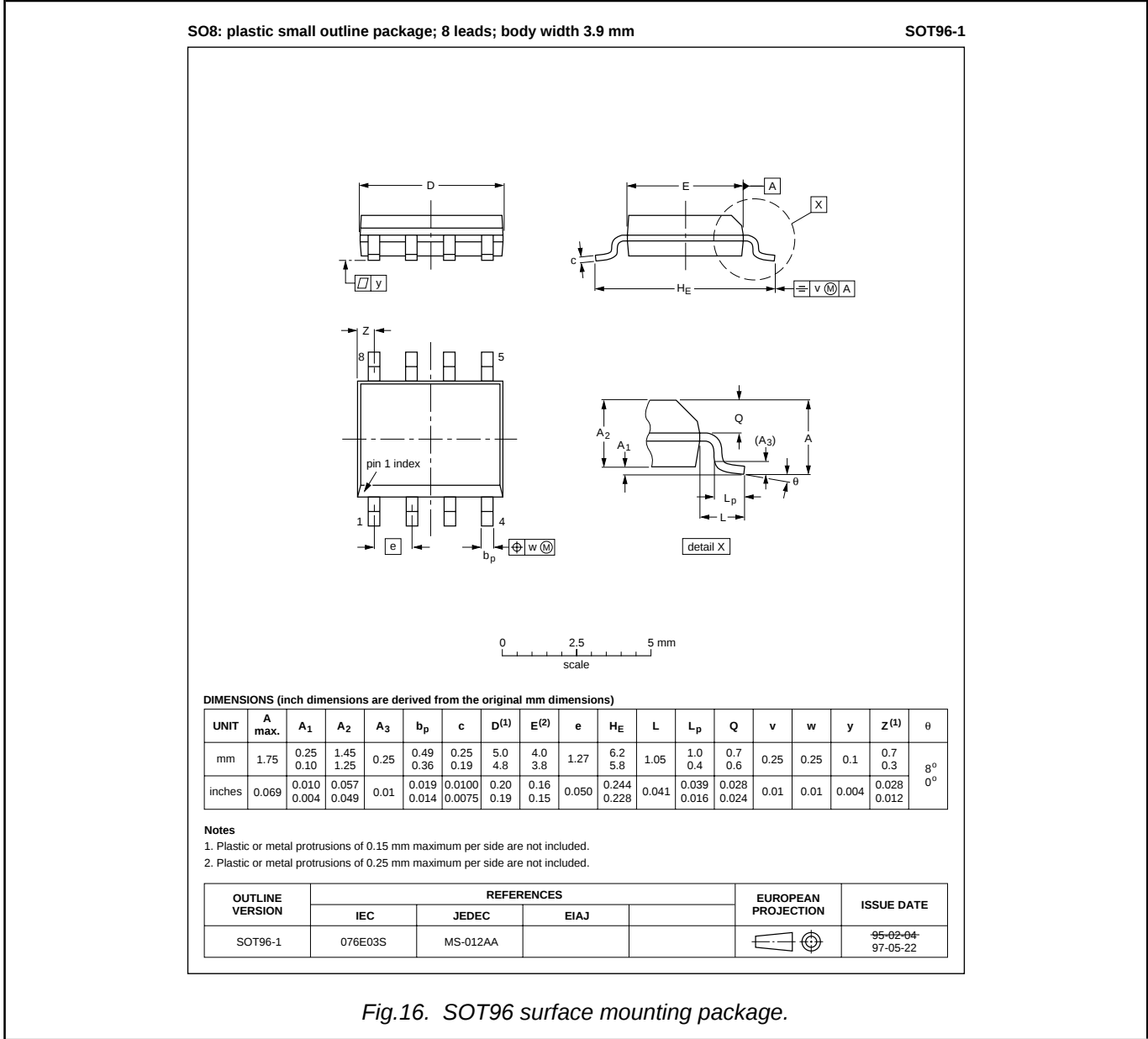


Fig.13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; parameter V_{DS}

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MECHANICAL DATA



Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to Integrated Circuit Packages, Data Handbook IC26.
3. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

DATA SHEET STATUS		
DATA SHEET STATUS ²	PRODUCT STATUS ³	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A
Limiting values		
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application information		
Where application information is given, it is advisory and does not form part of the specification.		
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